a third circuit to control a supply voltage of the first circuit; and

a fourth circuit to control a substrate bias voltage supplied to a semiconductor region where the at least one MOS transistor of the first circuit is formed,

wherein the frequency of the clock signal, the supply voltage and the substrate bias voltage are adjusted according to an operating performance of the first circuit,

wherein the operating performance of the first circuit includes at least an operating speed and a power consumption of the first circuit,

wherein at least one of the frequency of the clock signal, the supply voltage and the substrate bias voltage is set in order to satisfy a predetermined value of one of the operating speed and the power consumption of the first circuit; and

wherein at least one of a remaining two values of the frequency of the clock signal, the supply voltage and the substrate bias voltage are set in order to improve another of the operating speed and the power consumption of the first circuit.

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20. (Amended) The semiconductor integrated circuit device according to claim 17,

wherein one value of the frequency of the clock signal, the supply voltage and the substrate bias voltage is set in order to satisfy a predetermined operating speed, and

wherein a remaining two values of the frequency of the clock signal, the supply voltage and the substrate bias voltage are set in order to lower the power consumption of the first circuit.

21. (Amended) The semiconductor integrated circuit device according to claim 17,

wherein one value of the frequency of the clock signal, the supply voltage and the substrate bias voltage is set in order to satisfy a predetermined power consumption, and

wherein a remaining two values of the frequency of the clock signal, the supply voltage and the substrate bias voltage are set in order to increase the operating speed of the first circuit.

25. (Amended) A semiconductor integrated circuit device comprising:

a first circuit including at least one MOS transistor;

a monitor including at least one MOS transistor;

a second circuit to control a frequency of a clock signal to be supplied to the first circuit;

a third circuit to control a supply voltage of the first circuit;

a fourth circuit to control a substrate bias voltage supplied to a semiconductor region where the at least one MOS transistor of said first circuit is formed; and

wherein values of the frequency of the clock signal, the supply voltage and the substrate bias voltage value are set initially in order to satisfy an operating performance of the first circuit,

wherein the clock signal, the supply voltage and the substrate bias voltage are supplied to the monitor, and at least one value of the frequency of the clock signal, the supply voltage and the substrate bias voltage is controlled so as to reduce a delay between an output of the monitor and a reference signal,

wherein the operating performance of the first circuit includes at least an operating speed and a power consumption of the first circuit,

wherein at least one of the frequency of the clock signal, the supply voltage and the substrate bias voltage is initially set in order to satisfy a predetermined value of one of the operating speed and the power consumption of the first circuit; and

wherein at least one of a remaining two values of the frequency of the clock signal, the supply voltage and the substrate bias voltage are initially set in order to improve another of the operating speed and the power consumption of the first circuit.

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26. (Amended) The semiconductor integrated circuit device comprising:

a first circuit including at least one MOS transistor;

a monitor including at least one MOS transistor;

a second circuit to control a frequency of a clock signal to be supplied to the first circuit;

a third circuit to control a supply voltage of the first circuit;

a fourth circuit to control a substrate bias voltage supplied to a semiconductor region where the at least one MOS transistor of said first circuit is formed; and

wherein values of the frequency of the clock signal, the supply voltage and the substrate bias voltage value are set initially in order to satisfy an operating performance of the first circuit, based on predetermined combinations of the frequency of the clock signal and the substrate bias voltage according to the supply voltage, and

wherein the clock signal, the supply voltage and the substrate bias voltage are supplied to the monitor, and at least one value of the frequency of the clock signal,

the supply voltage and the substrate bias voltage is controlled so as to reduce a delay between an output of the monitor and a reference signal,

a comparator;

wherein the monitor is a delay circuit including inverters connected in series,

wherein the comparator compares an output of the monitor with the reference signal and outputs a first signal when the output of the monitor is later than the reference signal or a second signal when the reference signal is later than the output of the monitor, and

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wherein, when the first signal is outputted, the at least one value is controlled so that the operating speed of the first circuit is made faster, and, when the second signal is outputted, the at least one value is controlled so that the operating speed of the first circuit is made lower.

27. (Amended) A semiconductor integrated circuit device comprising:

a first circuit having a first MOS transistor of a first conductivity type and a second MOS transistor of a second conductivity type connected in series with the first MOS transistor; and

a second circuit to control substrate bias voltages supplied to semiconductor regions where the first and second MOS transistors are formed,

wherein said second circuit suppresses variations of an operating frequency of the first circuit by applying the substrate bias voltage,

wherein one of a frequency of a clock signal and a supply voltage of the first circuit, whose operating frequency variations are suppressed, are set in order to satisfy a predetermined value of one of the operating speed and the power consumption of. the first circuit; and

Cont B3

wherein another of the frequency of the clock signal and the supply voltage of the first circuit is set in order to improve another of the operating speed and. the power consumption of the first circuit.

Please **add** new claims 36-38 as follows:

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36. The semiconductor integrated circuit device according to claim 17,

wherein at least one of the frequency of the clock signal, the supply voltage and the substrate bias voltage is set by selecting one from combinations of at least two from the frequency of the clock signal, the supply voltage and the substrate bias voltage.

37. The semiconductor integrated circuit device according to claim 25,

wherein at least one of the frequency of the clock signal, the supply voltage and the substrate bias voltage is initially set by selecting one from combinations of at least two from the frequency of the clock signal, the supply voltage and the substrate bias voltage.

38. The semiconductor integrated circuit device according to claim 27,

wherein at least one of the frequency of the clock signal, the supply voltage and the substrate bias voltage is set by selecting one from combinations of at least two from the frequency of the clock signal, the supply voltage and the substrate bias voltage.